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PTO/SB/05 (4/98)

Approved for use through 09/30/2000. OMB 0651-0032

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<b>UTILITY PATENT APPLICATION TRANSMITTAL</b>	Attorney Docket No. 042390.P6958
(Only for new nonprovisional applications under 37 CFR 1.53(b))	First Inventor or Application Identifier Anne E. Miller
	Title HIGH pH SLURRY FOR CHEMICAL MECHANICAL POLISHING OF
	Express Mail Label No. EL034432535US

**APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents

1.  Fee Transmittal Form  
*(Submit an original, and a duplicate for fee processing)*
2.  Specification [Total Pages 21]  
*(preferred arrangement set forth below)*
  - Descriptive title of the Invention
  - Cross References to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to Microfiche Appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (*if filed*)
  - Detailed Description
  - Claim(s)
  - Abstract of the Disclosure
3.  Drawing(s) (35 U.S.C. 113) [Total Sheets 5]
4. Oath or Declaration [Total Pages 3]
  - a.  Newly executed (original copy)
  - b.  Copy from a prior application (37 C.F.R. § 1.63(d))  
*(for continuation/divisional with Box 16 completed)*
    - i.  DELETION OF INVENTOR(S)  
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

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5.  Microfiche Computer Program (Appendix)
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7.  Assignment Papers (cover sheet & document(s))
8.  37 C.F.R. § 3.73(b) Statement  Power of Attorney  
*(when there is an assignee)*
9.  English Translation Document (*if applicable*)
10.  Information Disclosure Statement (IDS)/PTO - 1449  Copies of IDS Citations
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P6958

PATENT

**HIGH pH SLURRY FOR CHEMICAL MECHANICAL POLISHING OF COPPER**

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Kenneth C. Cadien

"Express Mail" mailing label number EL034432535US

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## HIGH pH SLURRY FOR CHEMICAL MECHANICAL POLISHING OF COPPER

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Kenneth C. Cadieu

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### Background of the Invention

#### Field of the Invention

The present invention relates to the field of chemical mechanical polishing (CMP), and more specifically, to slurries and methods for chemical-mechanical polishing of metal.

#### Background

Advances in semiconductor manufacturing technology have led to the development of integrated circuits having multiple levels of interconnect. In such an integrated circuit, patterned conductive material on one interconnect level is electrically insulated from patterned conductive material on another interconnect level by films of material such as, for example, silicon dioxide. These conductive materials are typically a metal or metal alloy. Connections between the conductive material at the various interconnect levels are made by forming openings in the insulating layers and providing an electrically conductive structure such that the patterned conductive material from different interconnect levels are brought into electrical contact with each other. These electrically conductive structures are often referred to as contacts or vias.

Other advances in semiconductor manufacturing technology have lead to the integration of millions of transistors, each capable of switching at high

speed. A consequence of incorporating so many fast switching transistors into an integrated circuit is an increase in power consumption during operation. One technique for increasing speed while reducing power consumption is to replace the traditional aluminum and aluminum alloy interconnects found on integrated circuits with a metal such as copper, which offers lower electrical resistance. Those skilled in the electrical arts will appreciate that by reducing resistance, electrical signals may propagate more quickly through the interconnect pathways on an integrated circuit. Furthermore, because the resistance of copper is significantly less than that of aluminum, the cross-sectional area of a copper interconnect line, as compared to an aluminum interconnect line, may be made smaller without incurring increased signal propagation delays based on the resistance of the interconnect. Additionally, because the capacitance between two electrical nodes is a function of the overlap area between those nodes, using a smaller copper interconnect line results in a decrease in parasitic capacitance. In this way, replacing aluminum based interconnects with copper based interconnects provides, depending on the dimensions chosen, reduced resistance, reduced capacitance, or both.

As noted above, copper has electrical advantages, such as lower resistance per cross-sectional area, the ability to provide for reduced parasitic capacitance, and greater immunity to electromigration. For all these reasons, manufacturers of integrated circuits find it desirable to include copper in their products.

While advantageous electrically, copper is difficult to integrate into the process of making integrated circuits. As is known in this field, copper can adversely affect the performance of metal oxide semiconductor (MOS) field effect transistors (FETs) if the copper is allowed to migrate, or diffuse, into the transistor areas of an integrated circuit. Therefore copper diffusion

5 barriers must be used to isolate copper metal from those transistor areas. Additionally, unlike aluminum based metal interconnect systems which are formed by subtractive etch processes, copper interconnects are typically formed by damascene metal processes. Such processes are also sometimes referred to as inlaid metal processes. In a damascene process,  
10 trenches are formed in a first layer, and a metal layer is formed over the first layer including the trenches. Excess metal is then polished off leaving individual interconnect lines in the trenches. The removal of the excess copper is typically accomplished by chemical mechanical polishing (CMP). Although there are many known variations of the damascene method of  
15 metallization, the most common method for removing the excess copper metal is by CMP.

Accordingly, there is a need for CMP methods, materials, and apparatus to polish conductive materials such as copper.

20 **Summary of the Invention**

Briefly, a slurry for copper polishing has a pH between 7.5 an 12.

In a particular embodiment of the present invention, a slurry for polishing copper has a pH between 8 and 11.5, and includes a SiO<sub>2</sub> abrasive, an (NH<sub>4</sub>)<sub>2</sub>S<sub>2</sub>O<sub>8</sub> oxidizer, a benzotriazole corrosion inhibitor, and a K<sub>3</sub>PO<sub>4</sub>/K<sub>2</sub>HPO<sub>4</sub> buffer.

## **Brief Description of the Drawings**

Fig. 1 is a schematic cross-sectional view of a copper damascene structure. This structure represents a post-plating, pre-polishing state of fabrication.

5         Fig. 2 is a schematic cross-sectional view of the copper damascene  
structure of Fig. 1 after a conventional chemical mechanical polishing  
operation.

10         Fig. 3 is a schematic cross-sectional view of the copper damascene  
structure of Fig. 1 after a chemical mechanical polishing operation in  
accordance with the present invention.

       Fig. 4 is a flowchart showing the operations in a process of polishing a  
thin film in accordance with the present invention.

15         Fig. 5 is a Pourbaix diagram showing the domains of corrosion,  
immunity, and passivation of copper, at 25°C (after M. Pourbaix, *Atlas of  
Electrochemical Equilibria in Aqueous Solutions*, National Association of  
Corrosion Engineers, 1974, pg. 389).

### **Detailed Description**

20         A method and slurry for the chemical-mechanical polishing of copper  
are described. In the following description numerous specific details are set  
forth to provide an understanding of the present invention. It will be apparent,  
however, to those skilled in the art and having the benefit of this disclosure,  
that the present invention may be practiced with apparatus and processes  
that vary from those specified here.

25         **Terminology**

       The terms, chip, integrated circuit, monolithic device, semiconductor  
device or component, microelectronic device or component, and similar terms  
and expressions, are often used interchangeably in this field. The present  
invention is applicable to all the above as they are generally understood in  
30         the field.

- 5        The terms metal line, trace, wire, conductor, signal path and signaling medium are all related. The related terms listed above, are generally interchangeable, and appear in order from specific to general. In this field, metal lines are sometimes referred to as traces, wires, lines, interconnects or simply metal.
- 10      The terms contact and via, both refer to structures for electrical connection of conductors from different interconnect levels. These terms are sometimes used in the art to describe both an opening in an insulator in which the structure will be completed, and the completed structure itself. For purposes of this disclosure contact and via refer to the completed structure.
- 15      Design rules, as used herein, refers to a set of rules that define the width, spacing, and layer-to-layer relationships of the various elements that make up an integrated circuit. By way of example and not limitation, the minimum width of, and spacing between, interconnect lines on a particular interconnect level of an integrated circuit are specified in the design rules for any specific semiconductor manufacturing process.
- 20      Erosion, as used herein, refers to the amount of a layer, typically an interlayer dielectric, that is removed during the polishing of a metal damascene structure. Erosion is measured as a thickness, or distance, and more particularly, it is a measure of the distance between the original surface of the layer and its post-polish surface. Erosion is generally an undesirable result of overpolishing. The pre-polished thickness is shown as  $T_{ILD0}$  in Figure 1.
- 25      Examples of post-polish thickness can be seen in Figs. 2 and 3 and are identified as  $T_{ILD1}$  and  $T_{ILD2}$ . Erosion is defined as the total oxide loss represented by the differences,  $T_{ILD0} - T_{ILD1}$  and  $T_{ILD0} - T_{ILD2}$ . Typically, the erosion, or interlayer dielectric loss, is enhanced for structures such as serpentine, where the copper density is high relative to the dielectric density.

5       Recess, as used herein, refers to an amount of material, typically the metal of a metal damascene structure, that is removed during the polishing of the metal damascene structure. Recess is measured as a thickness, or distance, and more particularly, it is a measure of the distance between the post-polish surface of the interlayer dielectric and the post-polish surface of  
10 the metal. The recess is typically due to chemical attack rather than mechanical abrasion and is the main metal loss component of narrow, isolated metal lines. The spatial profile of a copper line due to recessing is typical flat. Examples of recess can be seen in Figs. 2 and 3 and are identified as  $T_{R1}$  and  $T_{R2}$ .

15      Dishing, as used herein, refers to an amount of material, typically the metal of a metal damascene structure, that is removed during the polishing of the metal damascene structure. Dishing is similar to recess in that it represents an overpolishing of the metal (i.e., excess material removal), however dishing typically results in a parabolic or concave shaped metal  
20 surface and is due to a mechanical interaction as the polish pad bends into the damascene structure. Dishing is measured as a thickness, or distance, and more particularly, it is a measure of the distance between the post-polish surface of the interlayer dielectric and the post-polish surface of the metal. Dishing typically occurs in metal structures that are wider than the minimum  
25 metal width permitted in a given set of design rules. Examples of dishing can be seen in Figs. 2 and 3 and are labelled as  $T_{D1}$  and  $T_{D2}$ .

The expression, low dielectric constant material, refers to a material having a lower dielectric constant than silicon dioxide.

Substrate, as used herein, refers to the physical object that is to be  
30 planarized by means of the CMP process. A substrate may also be referred to as a wafer. Wafers, may be made of semiconducting, non-semiconducting, or combinations of semiconducting and non-semiconducting

5 materials. Silicon wafers may have thin films of various materials formed upon them. These thin films may be planarized with CMP processing. Other substrate materials such as GaAs, silicon-on-sapphire, or silicon on insulator (SOI) may be planarized with CMP processing.

10 The term vertical, as used herein, means substantially perpendicular to the surface of a substrate.

RPM (also rpm) refers to revolutions per minute.

### Overview

15 Polishing of copper metal layers in connection with the formation of conductive interconnect lines for integrated circuits is becoming more important for the semiconductor industry. Unlike aluminum metallization, which is typically formed on integrated circuits by subtractive metal etch, copper interconnect lines are typically formed by way of a damascene, or inlaid, metal process. Such a process requires the removal, typically by chemical mechanical polishing (CMP), of the excess copper. CMP has been  
20 used successfully for polishing interlayer dielectrics such as silicon dioxide. CMP has also been used to polish metals such as tungsten, particularly in the formation of contact plugs. However, copper is unlike either silicon dioxide or tungsten. Copper is a soft metal compared to tungsten which makes CMP more difficult to achieve. As predicated by thermodynamics, both copper and  
25 tungsten slurries can be tailored for operation in the passivating pH regime of the Pourbaix diagram. Figure 5 shows the Pourbaix diagram for copper. In support of this theory, the bulk dissolution rate or static etch rate of slurries approach zero at pH > 6. However, in practice, the copper film that forms may be reactive with ionic species such as  $\text{SO}_4^-$  or  $\text{Cl}^-$ , and thus, benefits  
30 from the addition of a corrosion inhibitor such as benzotriazole. Erosion, dishing, and recessing are difficulties encountered in the CMP of copper because of the chemical and physical properties of copper.

5       Conventional methods of copper polishing for integrated circuit  
manufacturing include using an alumina-based, or silica-based, slurry at a pH  
equal to or less than 7.5. CMP of copper with conventional copper polish  
slurries frequently results in high corrosion rates. Furthermore, when  
conventional copper polish slurries are modified to include a corrosion  
10 inhibitor, the result is a narrow process window in terms of concentrations,  
pressures, and pad conditions, all of which limit the robustness, and in turn  
the cost effectiveness, of the copper polish process.

Furthermore, use of many of the conventional slurries, having an  
abrasive concentrations in the range of approximately 4% to 5%, results in  
15 the occurrence of glazing during the polishing of a wafer. Glazing refers to a  
condition wherein grooves, or other non-planarities, in the surface of a  
polishing pad fill up with particles or other material common to conventional  
copper polishing processes. Glazing reduces the ability of the polish pad to  
accomplish the desired material removal function. This phenomenon is  
20 sometimes referred to as shut-down. This can result in a requirement for  
longer polish times, or interim conditioning on CMP tools which do not include  
in-situ pad conditioning.

A copper polish slurry, in accordance with the present invention,  
operates with a high pH of greater than approximately 7.5. In this range the  
25 slurry has a low static etch due to formation of a robust, protective layer. This  
slurry may additionally have  $S_2O_8^{-2}$  or  $Fe(CN)_6^{-3}$  as an oxidizer and can thus  
offer a high polish rate on the order of 7,000 to 10,000 angstroms per minute.  
This polishing rate does not decrease significantly during polishing. Such an  
inventive slurry offers a wide CMP process window such that the slurry and  
30 process parameters can be optimized to yield low recess, erosion, and  
dishing on patterned wafers.

5 Various embodiments of the present invention offer a number of advantages over previous methods and slurries. Embodiments of the present invention offer negligible static etch rates. With the addition of a corrosion inhibitor in this pH regime, a stable, robust, passivating layer is formed on the copper, thereby providing a wide CMP process window in terms of  
10 concentrations, pad conditions, and polish pressures. Embodiments of the present invention provide an abrasive that substantially reduces or eliminates glazing, or shut down, during polish. Further embodiments of the present invention provide an abrasive that promotes high polish rates, and therefore high wafer throughput. Additionally, due to the substantial absence of  
15 glazing, a strong, robust, mechanical endpoint signature at polish pressures below 3 pounds per square inch (psi) is obtained. Because the polish rates enabled by embodiments of the present invention are substantially insensitive to pressure reduction, and can be operated effectively at polish pressures below 3 psi, erosion and dishing are both reduced. Furthermore, erosion can  
20 be tailored by reducing the SiO<sub>2</sub> concentration to below approximately 5% without inducing a significant reduction in polish rate. In a further aspect of the present invention, a buffer system that improves uniformity and reduces defects is provided.

25 The Slurry

An exemplary slurry, in accordance with the present invention, for chemical mechanical polishing of copper, has a pH between 8 and 11, and includes a SiO<sub>2</sub> abrasive, an (NH<sub>4</sub>)<sub>2</sub>S<sub>2</sub>O<sub>8</sub> oxidizer, a benzotriazole corrosion inhibitor, and a K<sub>3</sub>PO<sub>4</sub>/K<sub>2</sub>HPO<sub>4</sub> buffer.

30 An abrasive suitable for use in the embodiments of the present invention is a precipitated SiO<sub>2</sub>. This precipitated SiO<sub>2</sub> is preferred over a fumed, or gas phase, SiO<sub>2</sub>. Precipitated SiO<sub>2</sub> is sometimes referred to in this

- 5 industry as colloidal, although this term, i.e., colloidal, is not a technically accurate designation for this material.

In addition to  $(\text{NH}_4)_2\text{S}_2\text{O}_8$ , chemicals such as  $\text{K}_2\text{S}_2\text{O}_8$ , or  $\text{K}_3\text{Fe}(\text{CN})_6$  may be used as oxidizers.

- Corrosion inhibitors which may be used as an alternative to  
10 benzotriazole include other forms of benzotriazole such as 5-methyl benzotriazole or 1-methyl benzotriazole.

- In addition to the benzotriazole inhibitors, additional corrosion  
inhibitors containing  $\text{Ba}^{2+}$  or  $\text{Ca}^{2+}$  may be added to suppress the pitting  
corrosion that occurs in the presence of  $\text{S}_2\text{O}_8^{2-}$ . The addition of these cations  
15 getters  $\text{SO}_4^-$  species that otherwise attack the passive Cu-benzotriazole layer  
by forming an insoluble precipitate of either  $\text{BaSO}_4$  or  $\text{CaSO}_4$ .

Buffer systems which may be used as an alternative  $\text{K}_3\text{PO}_4/\text{K}_2\text{HPO}_4$   
include  $\text{KH}_2\text{PO}_4/\text{KOH}$ ,  $\text{K}_2\text{HPO}_4/\text{KOH}$ , and  $\text{KHCO}_3/\text{K}_2\text{CO}_3$

- In one embodiment of the present invention, a slurry includes 5 wt.%  
20 precipitated  $\text{SiO}_2$  as an abrasive, 0.05M  $(\text{NH}_4)_2\text{S}_2\text{O}_8$  as an oxidizer, 0.005M  
benzotriazole as a corrosion inhibitor, and 0.175g/l  $\text{K}_3\text{PO}_4$  and 0.046g/l  
 $\text{K}_2\text{HPO}_4$  as a buffer system. Alternative embodiments may include  $\text{SiO}_2$  in  
the range of 2 to 10 wt. %.

- Those skilled in the art and having the benefit of this disclosure will  
25 further recognize that it is not necessary to use a corrosion inhibitor, such as  
benzotriazole as part of the inventive slurry. Rather, this example is provided  
simply to illustrate the present invention. Those skilled in the art will further  
appreciate that a slurry formulated in accordance with the present invention  
will also include some reaction products of the various ingredients.

5    Method

In an embodiment of the present invention, a copper damascene structure is polished to form individual interconnects. Fig. 1 shows a copper damascene structure. An interlayer dielectric layer (ILD) is patterned to form ILD 102 on a surface of a wafer as illustrated in the figure. ILD 102 has a thickness represented by  $T_{ILD0}$  in Fig. 1. A copper diffusion barrier 104 is formed over the exposed surfaces of the wafer and ILD 102. Various materials may be used as the copper diffusion barrier. Tantalum and tantalum nitride are often proposed as advantageous copper diffusion barriers. Typically a copper seed layer is then formed on copper diffusion barrier 104. A complete copper layer 106 is then formed, typically by plating, over diffusion barrier 104.

Fig. 2 illustrates the results of conventional copper CMP. More particularly, erosion, recess, and dishing are all illustrated in the figure. The post-polish thickness of ILD 102 is shown as  $T_{ILD1}$ . The difference between  $T_{ILD0}$  and  $T_{ILD1}$  is called erosion. The erosion, (i.e.,  $T_{ILD0} - T_{ILD1}$ ) is typically measured in the center of a dense array such as a serpentine and is typically much greater than the erosion measured in a large open field. Recess, represented by  $T_{R1}$ , affects the thickness of the post-polish copper 106, and is measured from the top surface of the post-polish ILD 102 to the top surface of post-polish copper 106 as shown. Wide metal lines are particularly susceptible to a phenomenon known as dishing. Dishing, represented by  $T_{D1}$ , shows the additional material removed from wide metal lines.

Fig. 3 illustrates the results of copper CMP in accordance with embodiments of the present invention. Erosion, recess, and dishing are all illustrated in Fig. 3, but it can be seen that these exist to a lesser extent here than in Fig. 2. The post-polish thickness of ILD 102 in Fig. 3 is shown as  $T_{ILD2}$ . In Fig. 3 recess is represented by  $T_{R2}$ , and dishing is represented by  $T_{D2}$ . It can be seen that copper CMP in accordance with the present

5 invention produces a smaller erosion  $T_{ILD2}$ , recess  $T_{R2}$ , and dishing  $T_{D2}$ . This results in achieving the desired cross-sectional areas for copper interconnect. Table 1, below, shows the results obtained when polishing with a high pH slurry compared to a conventional slurry.

Table 1

Slurry	Conventional Slurry	High pH Slurry	High pH Slurry
pH	7.1	8.5	8.5
Pressure (psi)	3.75	3.75	2
Erosion (nm): 90% Copper Density	573	334	193
Dishing (nm): 100 $\mu\text{m}$ line	221	87	45
Recess (nm): 1 $\mu\text{m}$ line	41	3	0.5

10

An embodiment of the method of polishing a thin film on a wafer, in accordance with the present invention, is described in conjunction with Fig. 4.

As is well known, in a typical CMP system, a wafer is placed face down on a rotating table covered with a polishing pad, which has been coated 15 with a slurry. A carrier, which may be attached to a rotatable shaft, is used to apply a downward force against the backside of the wafer. A retaining ring may be used to center the wafer onto the carrier and to prevent the wafer from slipping laterally. By applying the downward force, and rotating the wafer, while simultaneously rotating a slurry covered pad, a desired amount 20 of material may be removed from the upper surface of a thin film on the surface of the wafer.

5        Fig.4 shows a flow diagram of a process embodying the present invention. At block **402**, a high pH slurry is prepared, delivered to, and dispensed onto, a polishing pad. The high pH slurry, as described above, is typically in the range of 7.5 to 12, and may be in the range of 8 to 11. Then, as shown at block **404**, a wafer with a copper damascene structure formed  
10 thereon, is brought into contact with the polishing pad. As shown at block **406** the copper damascene structure is polished. Typical polishing conditions using an orbital polisher are a down force of approximately 3.75 psi, an orbital speed of approximately 310 rpm, a wafer rotational speed of approximately 10 rpm, a slurry flow rate of 200 ccm, and delta P of -0.1 psi. Delta P is the  
15 pressure difference exerted on the top and bottom of the wafer and allows fine control of the rate at the edge of the wafer. Stacked polishing pads such as the IC1000, with a Suba-4 sub-pad, both made by Rodel, Inc. of Newark, Delaware, can be used with the high pH slurry to polish copper films. FX-9 pads from Freudenberg of Lowell, Massachusetts, can be also used.  
20 Removal rates of approximately 8505 angstroms per minute have been obtained with within wafer non-uniformity (1 sigma) of 6.5%.

Copper diffusion barriers, such as, for example, tantalum or tantalum nitride, are also successfully polished with slurries and polishing conditions in accordance with the present invention.

25        Methods and slurries in accordance with the present invention may be used with various interlayer dielectric materials. For example, even though SiO<sub>2</sub> has traditionally been the dielectric material used between interconnect levels on integrated circuits, various low-k dielectric materials, including but not limited to, SiOF may also be used with embodiments of the present  
30 invention.

The motor current endpoint signal obtained with embodiments of the present invention are stronger than those found with conventional copper

- 5      CMP processes. This improved mechanical endpoint correlates with the absence of glazing.

Conclusion

Embodiments of the present invention provide high pH slurries for chemical mechanical polishing of copper films.

- 10     An advantage of some embodiments of the present invention is that the polish time can be reduced thus reducing manufacturing cost.

A further advantage of some embodiments of the present invention is that dishing is reduced.

- 15     A still further advantage of some embodiments of the present invention is that erosion is reduced.

A still further advantage of some embodiments of the present invention is that the polish end point signal is improved as compared to that obtained in conventional methods.

- 20     It will be apparent to those skilled in the art that a number of variations or modifications may be made to the illustrative embodiments described above. For example, various combinations, slurry pH, slurry delivery rate, pad rotation speed, pad temperature, and so on, may be used within the scope of the present invention.

- 25     Other modifications from the specifically described apparatus, slurry, and process will be apparent to those skilled in the art and having the benefit of this disclosure. Accordingly, it is intended that all such modifications and alterations be considered as within the spirit and scope of the invention as defined by the subjoined Claims.

What is claimed is:

1    1.    A method of forming copper interconnect, comprising:  
2       forming a dielectric layer over a substrate, the dielectric layer having  
3       trenches therein;  
4       forming a copper diffusion barrier at least in the trenches;  
5       depositing copper over the copper diffusion barrier and over a top surface  
6       of the dielectric layer; and  
7       polishing the copper with a high pH slurry;

1    2.    The method of Claim 1, wherein the dielectric layer comprises an oxide of  
2       silicon, and the copper diffusion barrier is electrically conductive.

1    3.    The method of Claim 1, wherein the dielectric layer comprises a  
2       fluorinated oxide of silicon, and the copper diffusion barrier is selected from the  
3       group consisting of tantalum, and tantalum nitride.

1    4.    The method of Claim 1, wherein the high pH slurry has a pH between  
2       approximately 7.5 and 12.

1    5.    The method of Claim 4, wherein the high pH slurry has a pH between  
2       approximately 8 and 11.5.

1    6.    The method of Claim 1, wherein the slurry contains approximately 2% to  
2    10% by weight of SiO<sub>2</sub>.

1    7.    The method of Claim 1, wherein the slurry contains an oxidizer comprising  
2    (NH<sub>4</sub>)<sub>2</sub>S<sub>2</sub>O<sub>8</sub>.

1    8.    The method of Claim 1, wherein polishing comprises chemical mechanical  
2    polishing with a down force of less than or equal to approximately 3.75 psi.

1    9.    The method of Claim 1, wherein polishing comprises:  
2        engaging the copper with a polishing pad with a down force less than or  
3        equal to 3.75 psi; and  
4        providing a slurry flow rate of approximately 200 ccm.

1    10.   The method of Claim 9, wherein polishing further comprises an orbital  
2        speed of approximately 310 rpm and a wafer rotational speed of approximately  
3        10 rpm.

1    11.   A method of polishing a film, comprising:  
2        polishing the film with a slurry having a pH in a range such that a  
3        protective layer is formed over the film during polishing.

1    12.    The method of Claim 11, wherein the film comprises copper and the pH is  
2    the range of approximately 8 to 11.5.

1    13.    The method of Claim 12, wherein the slurry comprises a precipitated SiO<sub>2</sub>.

1    14.    The method of Claim 13, wherein the precipitated SiO<sub>2</sub> comprises  
2    approximately 2 to 10 wt.% of the slurry.

1    15.    A slurry, comprising:  
2         an abrasive comprising precipitated SiO<sub>2</sub>;  
3         an oxidizer;  
4         a corrosion inhibitor; and  
5         a buffer system;  
6         wherein the slurry has a pH between 8 and 11.5.

1    16.    The slurry of Claim 15, wherein the abrasive is approximately 5 wt.%  
2    precipitated SiO<sub>2</sub>.

1    17.    The slurry of Claim 15, wherein the oxidizer comprises (NH<sub>4</sub>)<sub>2</sub>S<sub>2</sub>O<sub>8</sub>.

1    18.    The slurry of Claim 17, further comprising reaction products of  
2    (NH<sub>4</sub>)<sub>2</sub>S<sub>2</sub>O<sub>8</sub>.

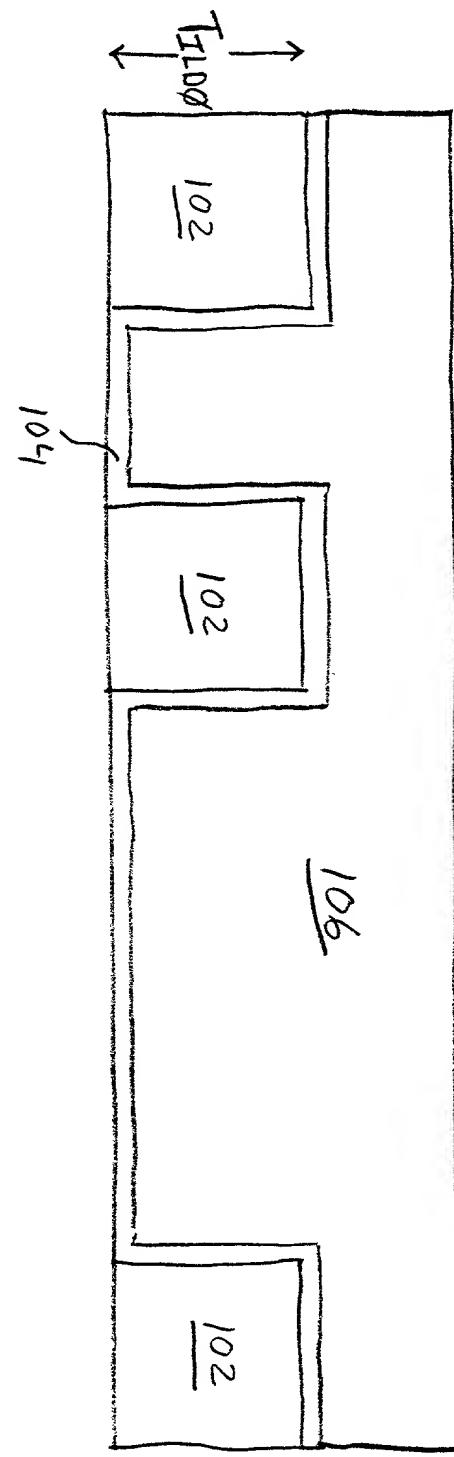
- 1    19.    The slurry of Claim 15, wherein the oxidizer comprises  $K_2S_2O_8$ .
- 1    20.    The slurry of Claim 19, further comprising reaction products of  $K_2S_2O_8$ .
- 1    21.    The slurry of Claim 15, wherein the oxidizer comprises  $K_3Fe(CN)_6$ .
- 1    22.    The slurry of Claim 21, further comprising reaction products of  $K_3Fe(CN)_6$ .
- 1    23.    The slurry of Claim 15, wherein the corrosion inhibitor comprises  
2    benzotriazole.
- 1    24.    The slurry of Claim 15, wherein the buffer comprises  $K_3PO_4$  and  $K_2HPO_4$ .
- 1    25.    The slurry of Claim 18, further comprising a getter such as  $Ba(OH)_2$ .
- 1    26.    The slurry of claim 20 further comprising a getter such as  $Ba(OH)_2$ .
- 1    27.    A slurry comprising:  
2        water;  
3        approximately 5 wt. % precipitated  $SiO_2$ ;  
4        approximately 0.05 M  $(NH_4)_2S_2O_8$ ;  
5        approximately 0.005 M benzotriazole; and

6        a buffer comprising approximately 0.175 g/l K<sub>3</sub>PO<sub>4</sub> and approximately  
7    0.046 g/l K<sub>2</sub>HPO<sub>4</sub>;  
8        wherein the slurry has a pH between approximately 8 and 11.5.

## ABSTRACT OF THE DISCLOSURE

A slurry for copper polishing has a pH between 7.5 and 12. In a particular embodiment of the present invention, a slurry for polishing copper has a pH between 8 and 11.5, and includes a SiO<sub>2</sub> abrasive, a (NH<sub>4</sub>)<sub>2</sub>S<sub>2</sub>O<sub>8</sub> oxidizer, a benzotriazole corrosion inhibitor, and a K<sub>3</sub>PO<sub>4</sub>/K<sub>2</sub>HPO<sub>4</sub> buffer. A copper polish slurry, in accordance with the present invention, operates with a high pH of greater than approximately 7.5. In this range the slurry has a low static etch due to formation of a robust, protective layer. This slurry may additionally have S<sub>2</sub>O<sub>8</sub><sup>-2</sup> or Fe(CN)<sub>6</sub><sup>-3</sup> as an oxidizer and can thus offer a high polish rate on the order of 7,000 to 10,000 angstroms per minute which does not decrease significantly during polishing. Such an inventive slurry offers a wide CMP process window such that the slurry and process parameters can be optimized to yield low recess, erosion, and dishing on patterned wafers.

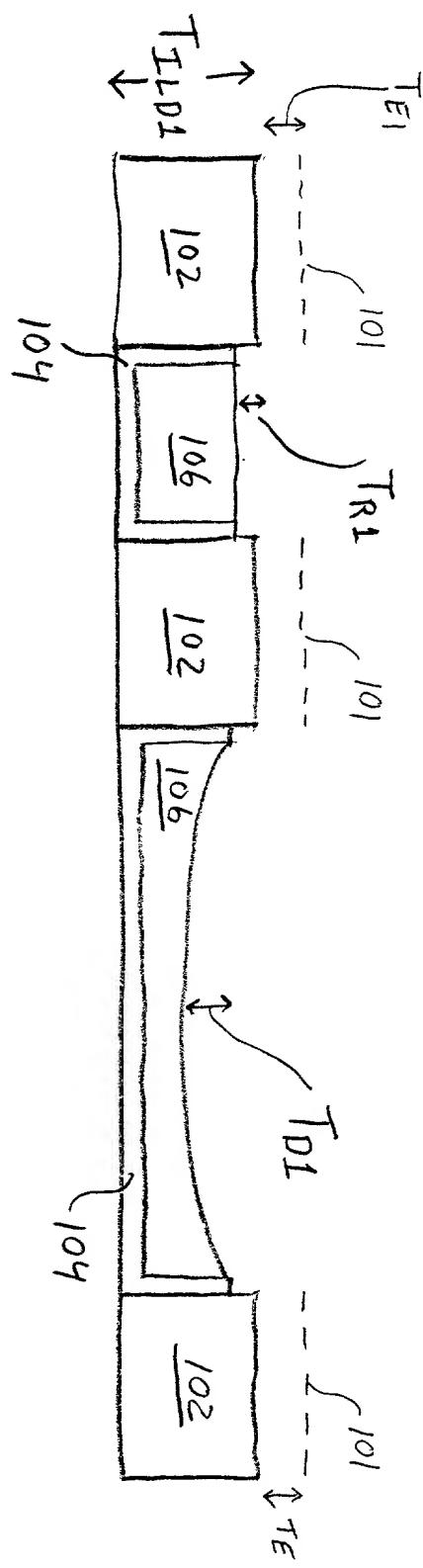
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Fig. 2



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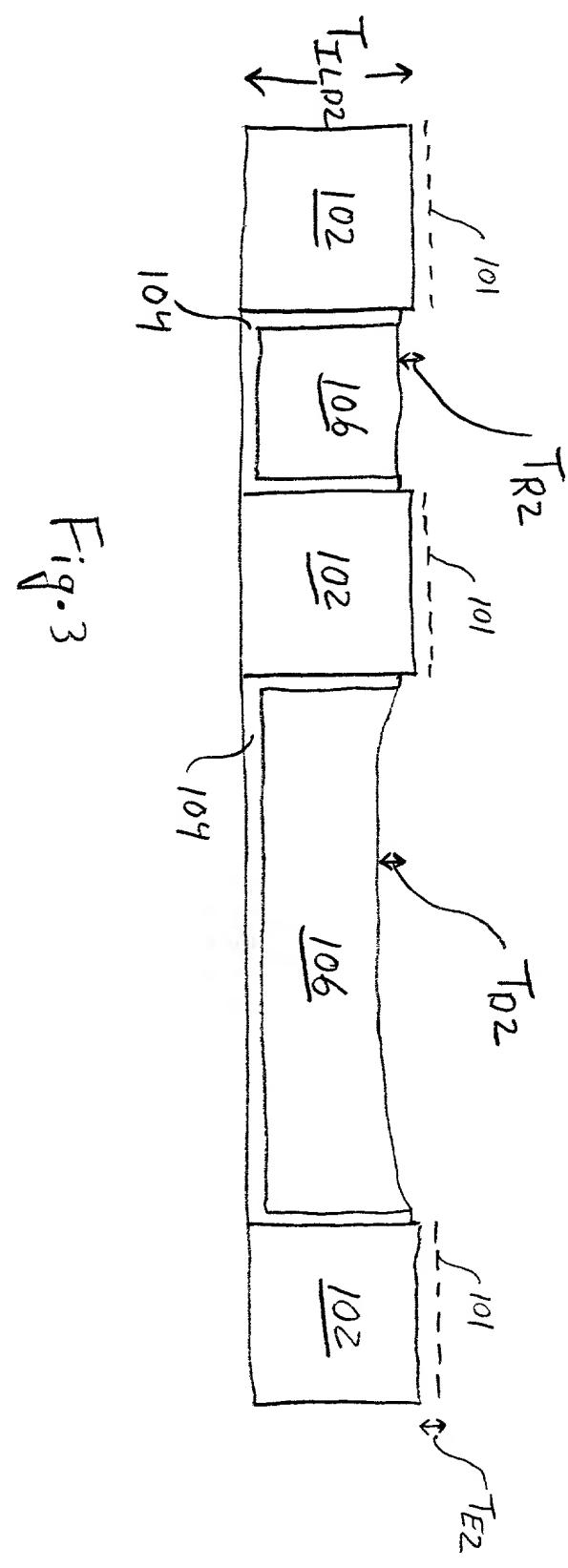


Fig. 3

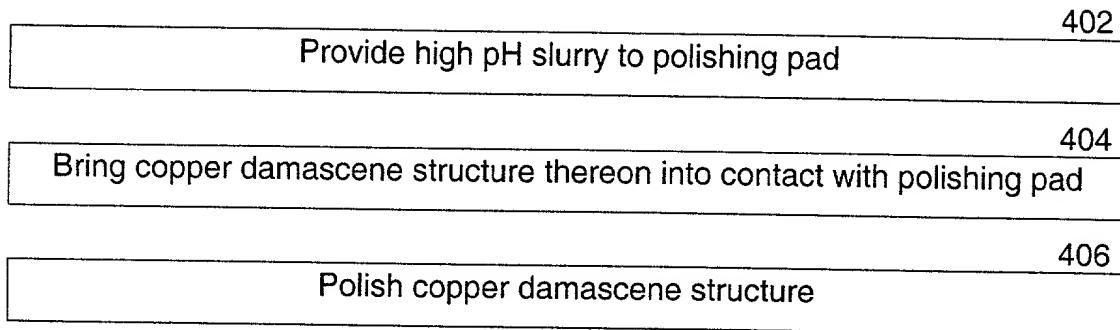
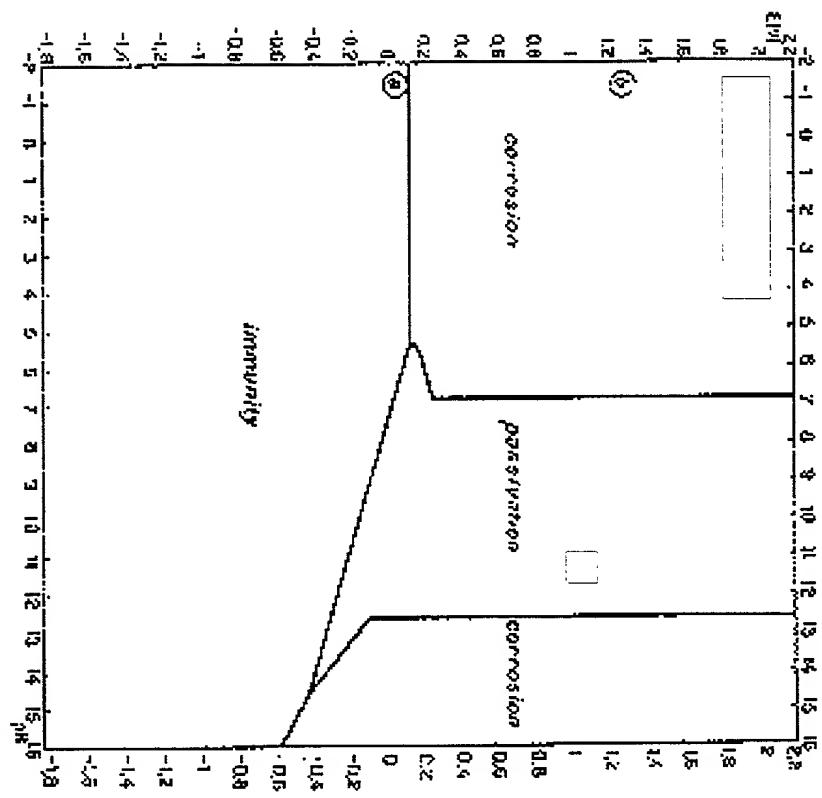


Fig. 4

Fig. 5



**DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION  
(FOR INTEL CORPORATION PATENT APPLICATIONS)**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

**HIGH pH SLURRY FOR CHEMICAL MECHANICAL POLISHING OF COPPER**

the specification of which

is attached hereto.  
 was filed on \_\_\_\_\_ as \_\_\_\_\_  
 United States Application Number \_\_\_\_\_  
 or PCT International Application Number \_\_\_\_\_  
 and was amended on \_\_\_\_\_  
 (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 37 USC 119
			<input type="checkbox"/> No <input type="checkbox"/> Yes
			<input type="checkbox"/> No <input type="checkbox"/> Yes
			<input type="checkbox"/> No <input type="checkbox"/> Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature \_\_\_\_\_ Date \_\_\_\_\_

Residence \_\_\_\_\_ Citizenship \_\_\_\_\_  
*(City, State)* *(Country)*

P. O. Address \_\_\_\_\_